Electronics status

Andrei Nomerotski 5/15/2003

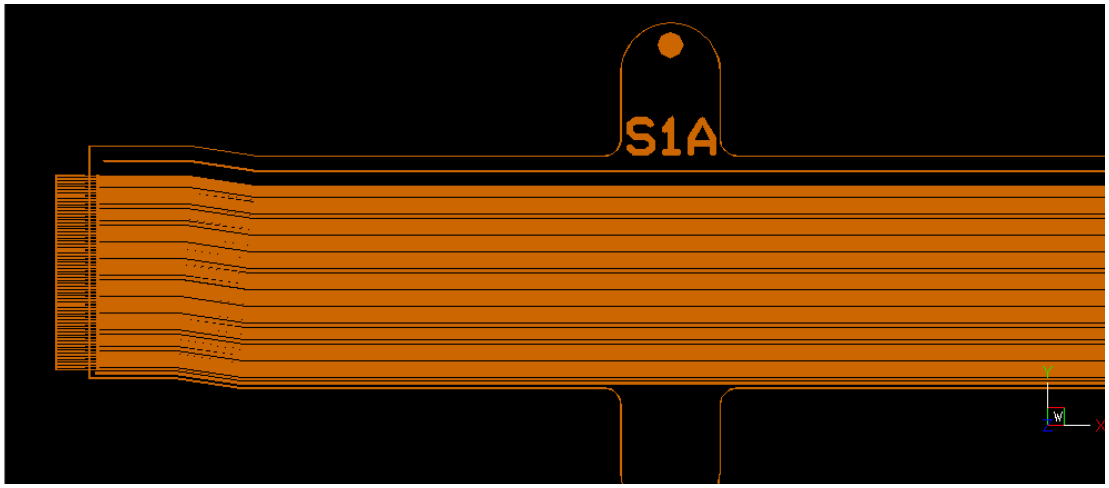
- SVX4 chip
- Analog flex cable
- Hybrids
- Modules
- Purple/Junction/Adapter Card
- Jumper/Twisted Pair Cables
- Teststands

SVX4 Chip

- Last ½ year busy with yield/hybrid/firmware/full chain tests (Mike U, Sara L, Sergey B, Kristian H, Kazu H)
- Verification of rev.2 SVX4 design/simulations (Len C, Petros R, Marvin J)
- Rev.2 chips ordered end of March, received this week
- 25 wafers x 300 chip/wafer x yield /(CDF+D0) = ~ 3 k chips for D0 (SMT2 total 7440, budgeted 15 k)
- Testing plans
  - First non-tested chips available in 1-2 weeks
  - First wafer tested chips available in 3-4 weeks
  - Will test single chips asap at 14th floor (LBL and stimulus setups)
  - Will stuff a few L0 hybrids asap with untested chips, stuff more hybrids as tested chips appear
- SVX4 manual (Len C, Petros R), see
  - http://d0server1.fnal.gov/users/Rapidis/manual.html

L0 Analog Cables

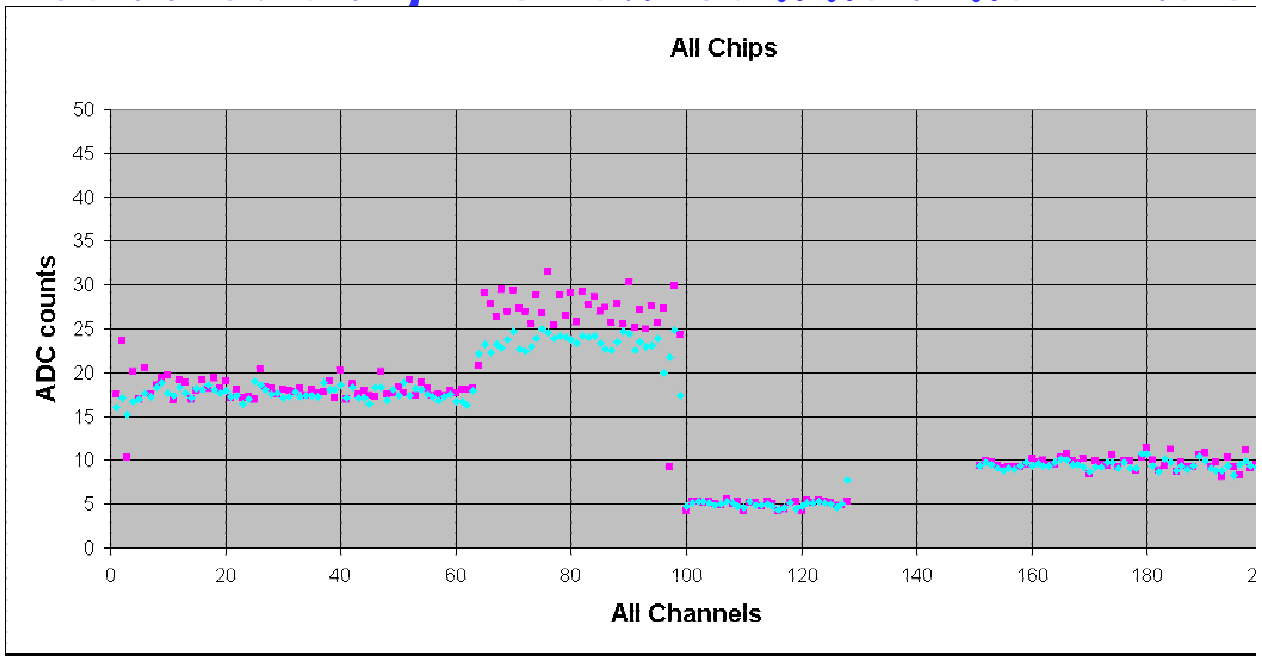
- Received 40 new cables in March 03, all good
- Trace width 19 um, capacitance 0.35 pF/cm (Frank L, Kazu H)
- Dyconnex trying lamination of 2 cables with kapton mesh as spacer and ceramic piece to support bonding



- See details in
  - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/L0/dyconex_status_march2k3.pdf

L0 module

- Noise studies with L0 structure (Kazu H, Daekwang)
  - Noise vs. two cables separation
  - Shielding/Grounding effects
  - Noise vs. distance to shielding
- Low inductance connection gives low common mode noise



- See details in
  - http://d0server1.fnal.gov/users/kazu/www/smt2b/meetingUW.pdf

Hybrids

- L2A & L2S hybrids (10 chips)
  - Received total 74 hybrids from Amitron and CPT
  - Electrically tested ~ 50 (Peter B, Juan H, Alice B, other KU)
  - Stuffed 31 (18 OK, 6 unknown) (Ray H.)
    - 9 last hybrids stuffed with tested chips all OK
  - All testing locations have working hybrids
  - Assembled 6 modules (4 OK)
  - See details in
    - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/Hybrids/Hybrids_AN050503.pdf
- Rev.2 hybrids
  - Testing of rev.1 finished in February 2003
  - rev.1-rev.2 changes reviewed in
    - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/Hybrids/Hybrids_AN022403.pdf
  - Layout of rev.2 ready in May 2003, see L2A in
    - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/Hybrids/L2-5hybrid/L2A_042503/L2A_042503.pdf
  - Received quotes from 6 vendors

Hybrid Flatness

- Original specification for flatness was 50 um
  - Not perfect CTE matching of BeO and dielectric (including different temperature dependence) causes bending during firing cycles – known effect
  - To compensate some dielectric is printed on the other side of BeO substrate
    - Limitations : Total thickness spec (0.95 mm) and processing issues
  - Another approach tried by CPT is lapping
- Three first batches from CPT were close to the spec while two last batches failed
  - Reason not understood, apparently 50 um spec is too tight
- After discussions with mechanical group decided to increase the flatness spec to 150 um
  - Gluing to silicon is less trivial but possible – tests successful
  - Hybrid temperature ok even with partial glue coverage (up by 2 degC)

Flatness (2)

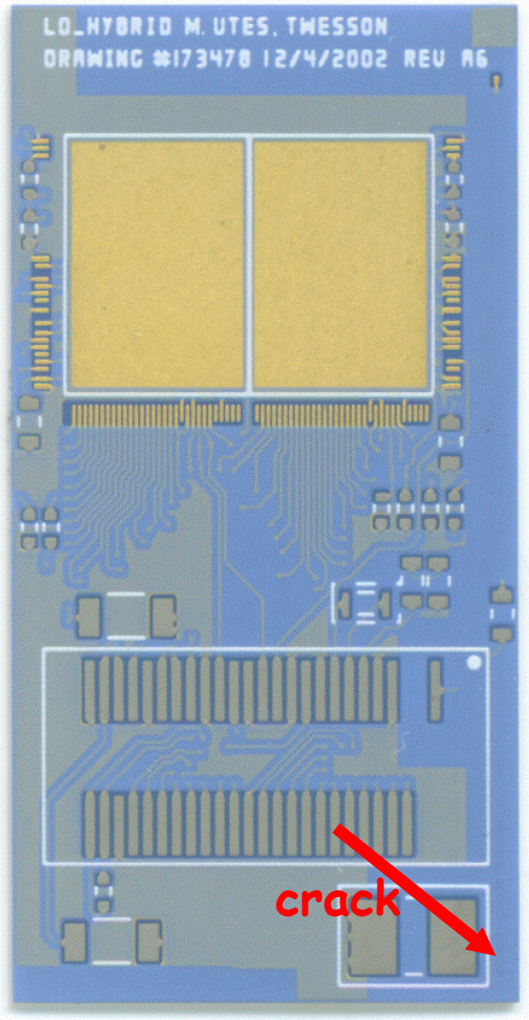
- Summary table

	Flatness	Thickness	Recess depth
CPT L2A 1	60	970	110
CPT L2S 1	45	940	100
CPT L2A 2	120	1000	30
CPT L2S 2	80	930	60
CPT L1	40	920	100
Amitron L2A	190	840	40

- In touch with CPT and Amitron on flatness issue – they believe the new spec is doable with some safety margin
- In any case this is a concern and more vendors are being contacted, probably will order samples from two more vendors

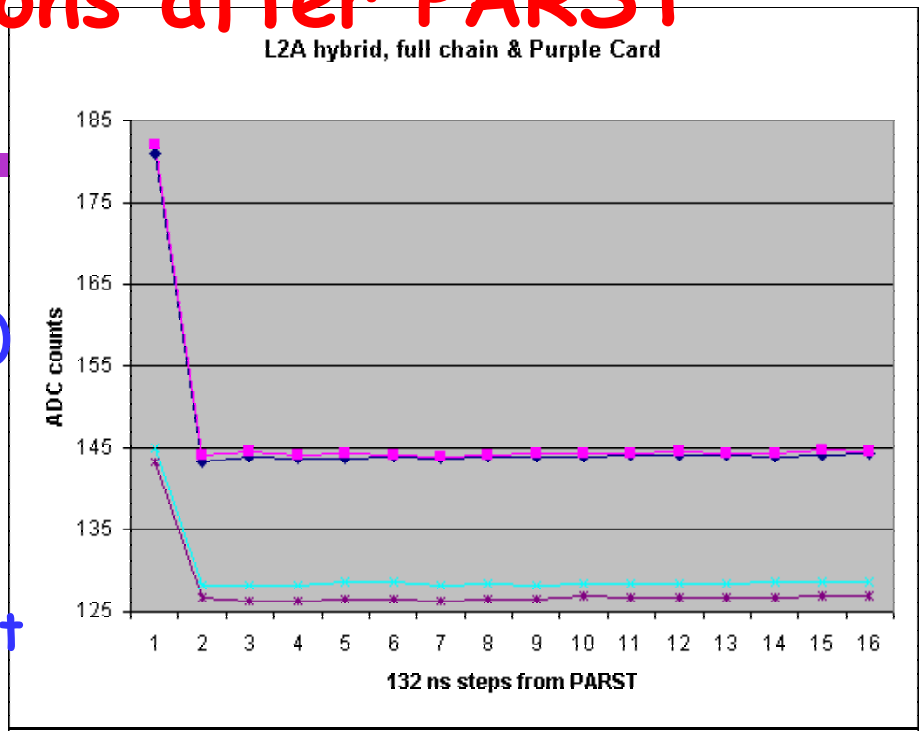
L0 hybrids

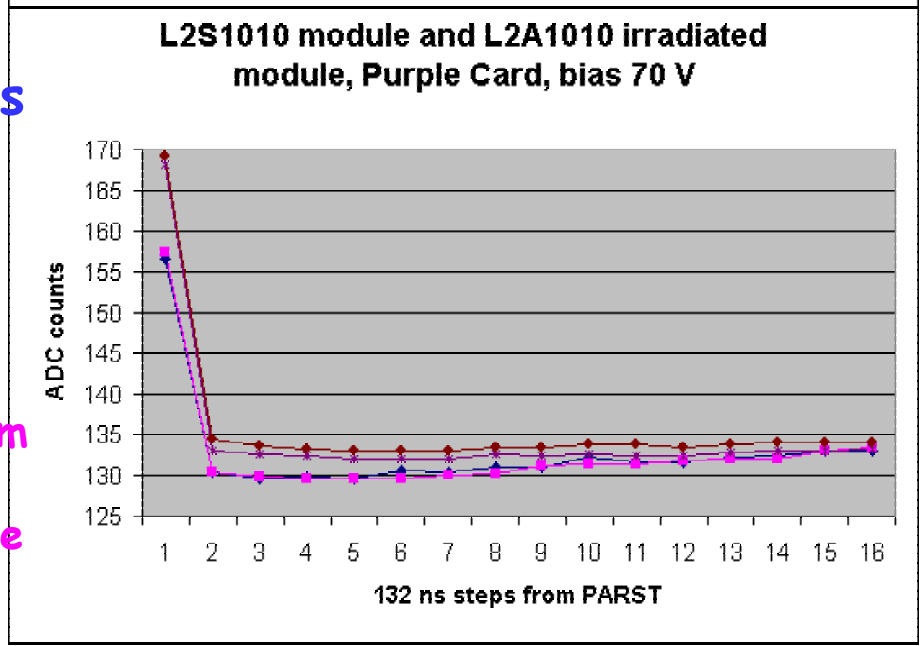
- 50 hybrids did not pass Amitron QA
  - A few mm crack in the corner during dicing
  - Electrical tests ok
  - Amitron started new lot
- Received 22 hybrids for free, inspected two
  - Crack ~10 micron
  - Does not cross artwork
  - Dimensions are ok
    - Flatness 20-40 um (spec 100 um)
    - Thickness 750 um (spec 800 um)
- Can be used for L0 prototypes
  - will stuff several hybrids



Oscillations after PARST

- In SMT see ~ 2 ADC counts oscillations as function of distance to PreamReset (PARST)
  - May be coming from GND oscillation – reason of concern and recent discussions
- Bare SVX4 measurements does not see this (see Kazu's slides at 2/24/2003 meeting)
- Done measurements addressing this for 10-chip hybrids/modules
  1. With Purple Card (top curves)
  2. With full chain (bottom curves)
  3. For non-irradiated and irradiated module
  - No oscillation seen
  - Slope 1-2 ADC counts expected from the pipeline slope
  - Irradiated module had 3 counts slope – investigating



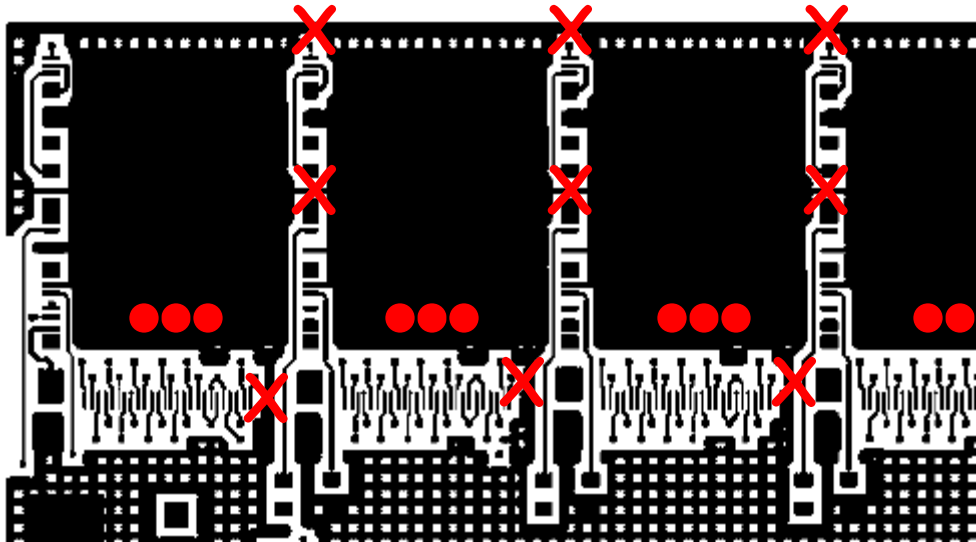


Changes in Hybrid Ground

- Reviewed ground configuration for rev.2 hybrids (J.Anderson, M.Johnson, M.Utes, J.Green, AN)
  - Before had a common ground allowing for digital currents under SVX4 chips
  - Single point analog and digital ground connection near SVX4 is best theoretically. For multi-ADC design the implementation is less straightforward but in any case maximum isolation of analog ground is recommended.
  - Decided to modify hybrid top metal layer to isolate analog ground of each chip (following H.Johnson's recipe on multiple ADC grounding) and also to provide low inductance pass for digital ground by multiple bond connections.

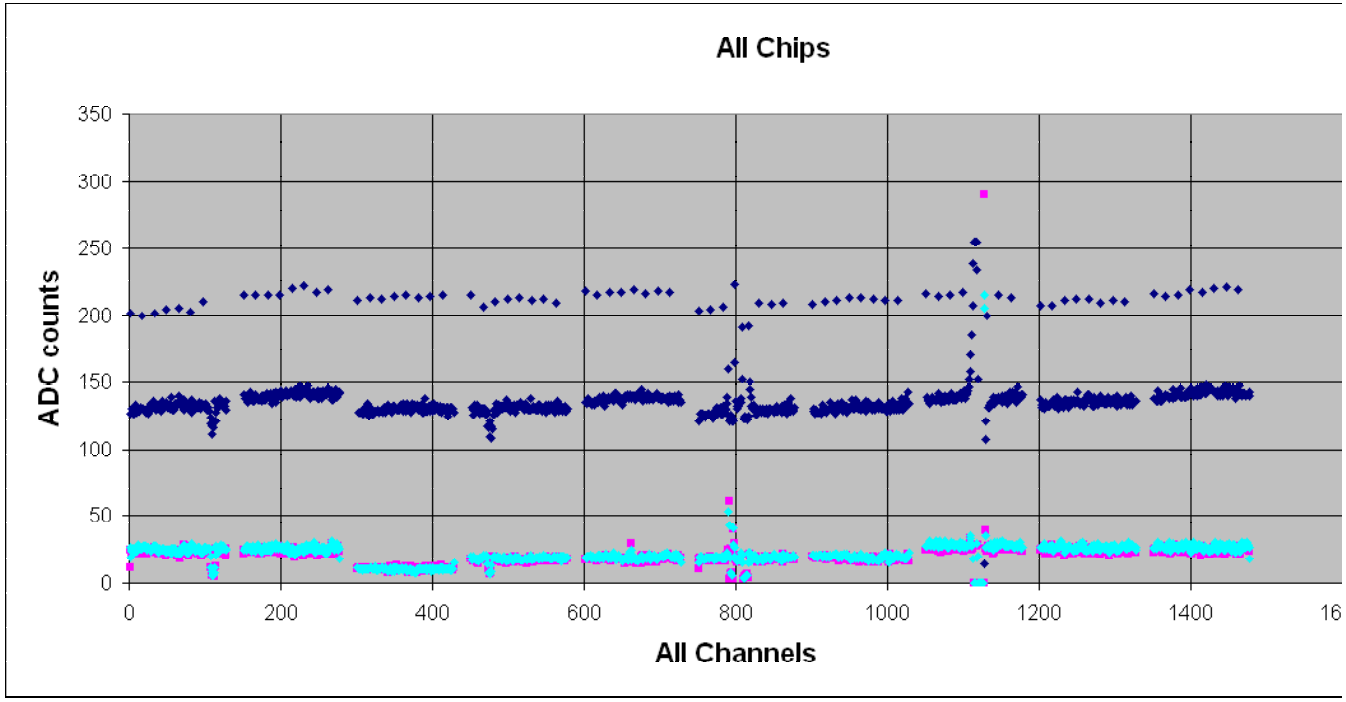
Changes :

1. Break ground bridges between chips and from chips to mesh ground (red crosses)
2. Have 3 vias (red dots) from the chip ground to ground plane (last metal layer)
3. Bond digital grounds from both sides of SVX4



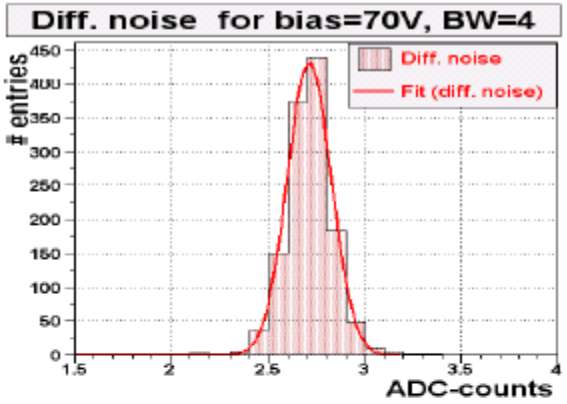
Module testing

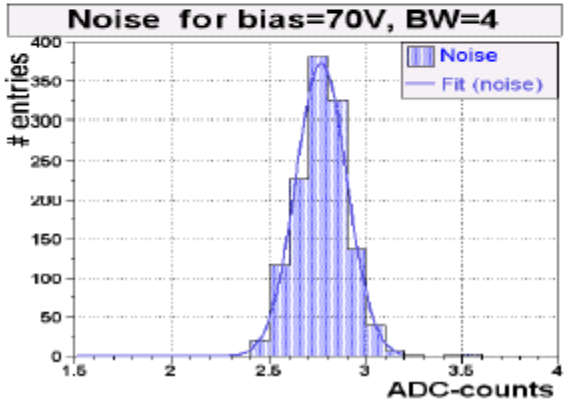
- Have 6 L2A/L2S, 1 L1 and 5 L0 modules, several more in the production pipeline
- Have good noise performance, see laser etc, (Gustavo O, Sara L, Ike H) details in
  - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/ModuleTesting/ModuleTesting_AN021703.pdf
  - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/Teststand/Teststand_GO120902.ppt

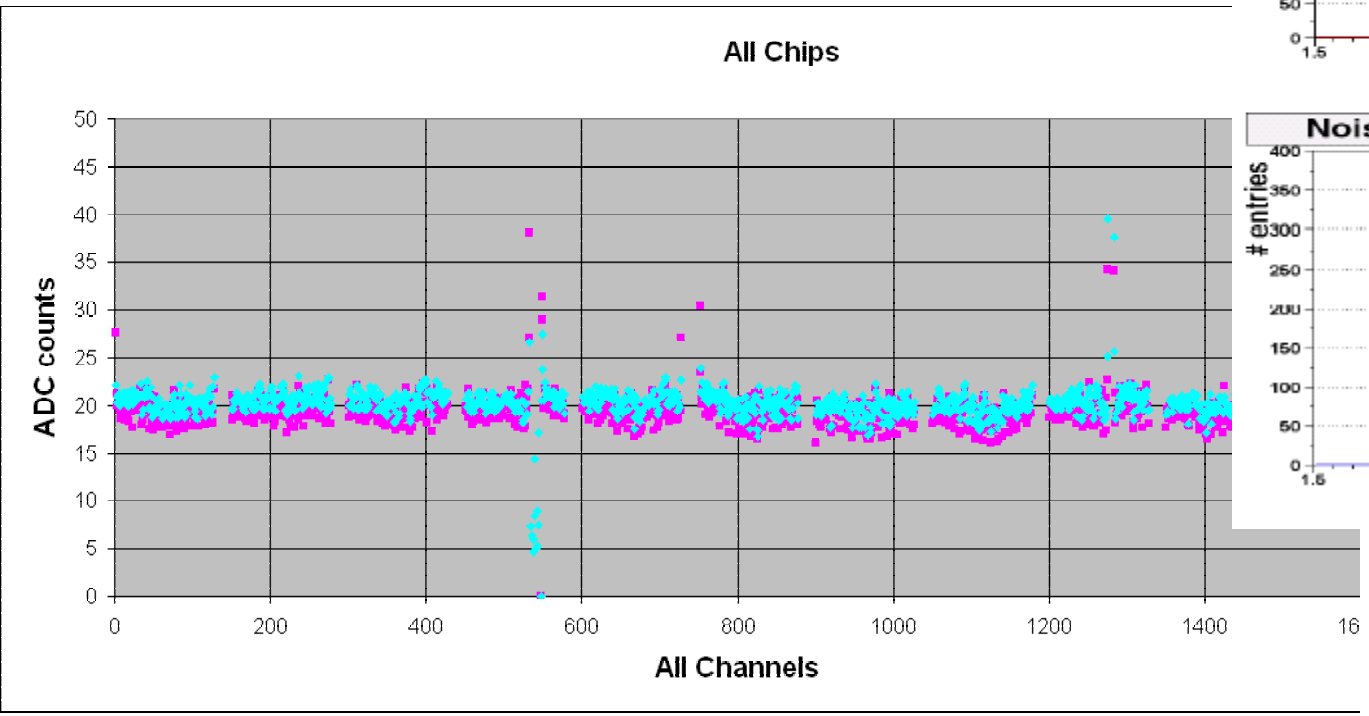


Irradiated module

- Studied shot noise in irradiated module (Daniela K, AN)
  - Temperature dependence
  - BW dependence
  - In process of refining measurements + integration time study

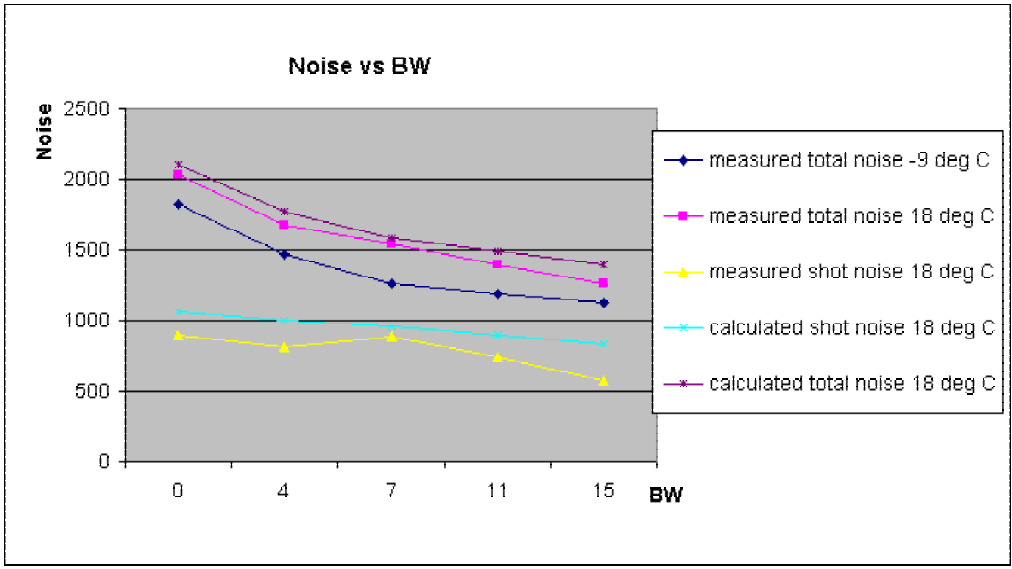






Irradiated module

- See reasonable agreement with calculation, correct BW dependence, see details in
  - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/ModuleTesting/ModuleTesting_AN031703.pdf
  - http://www-clued0.fnal.gov/~kaefer/analysis/irrmod_l2a1010_7_12may03.pdf

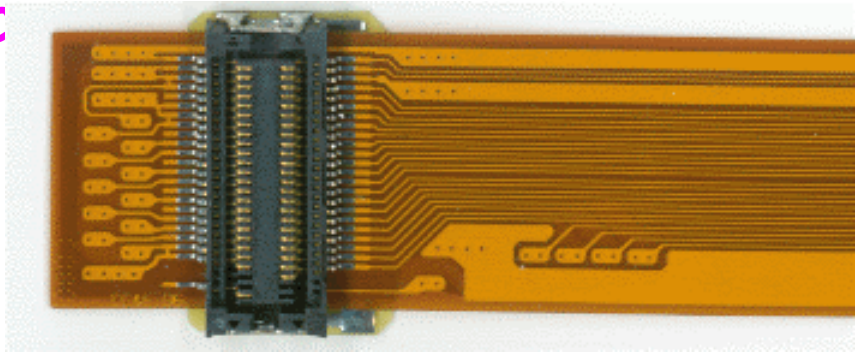


- Other urgent tasks in module testing
  - Sensor vs. Module comparison – nobody is working on this
  - Module (and hybrid) burn-in – slowly coming along

Digital Jumper Cable

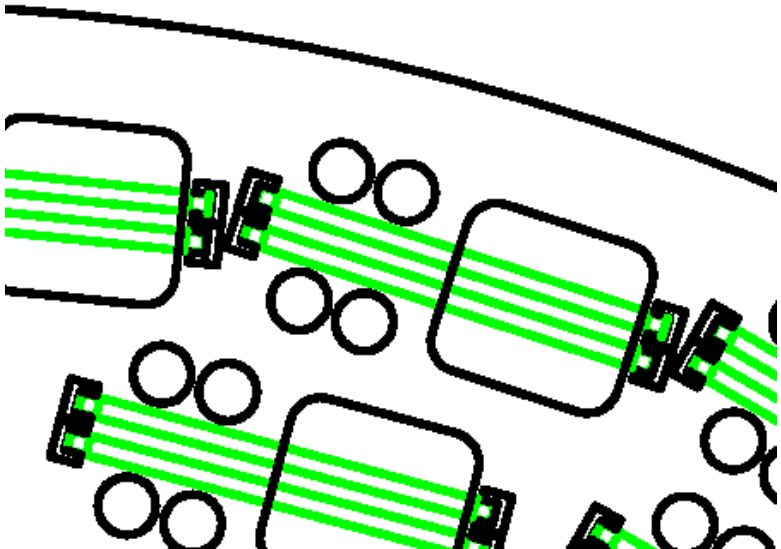
Hybrid - **Jumper Cable** - Junction Card - Twisted Pair Cable – Adapter Card

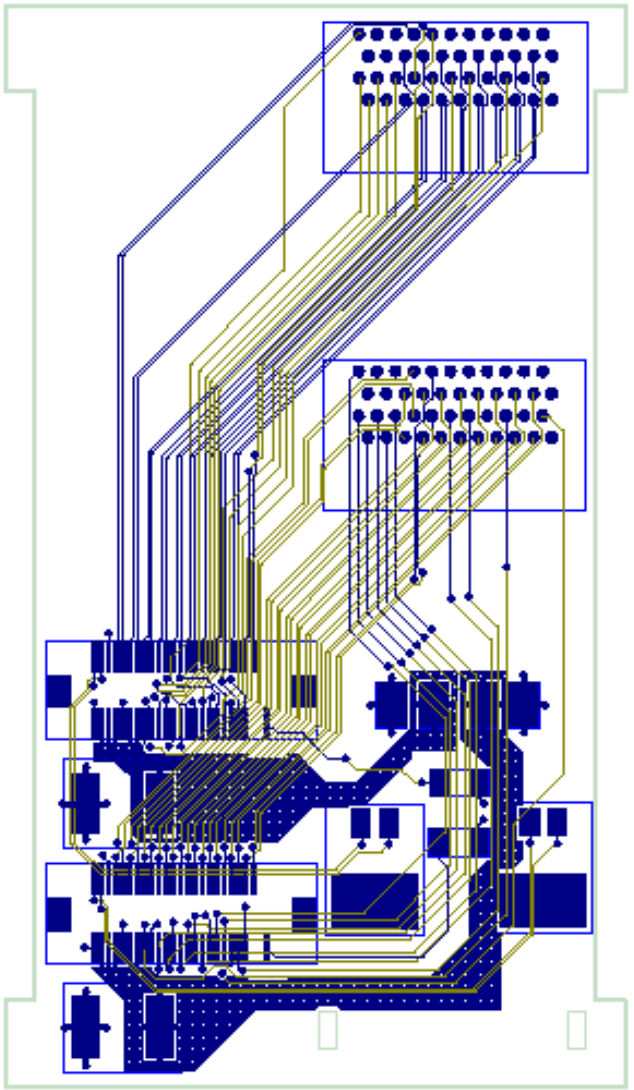
- Will use 2.5 mm connector on hybrid end, 3 mm connector with strain relief on JC end
- Ordered 450 teststation cables
  - Received 300 from Century
  - Currently going through production steps
    - 150 being ablated
    - 150 connectors installed, waiting for backing
- Backing
  - Agreed with mechanical group on 17x12x0.25 mm dimensions, see
    - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/JumperCable/DJC_032403.pdf
  - Want to use soldering to strain relief pads
  - Received prototypes – testing (C



Junction card

- Changed design : soldering -> connector for signal twisted pair cables
- Max dimensions 75 x 45 mm
- 3 types of JC
  - L2-5_top 2 channels
  - L2-5_bottom 2 channels
  - L0-1 3 channels
- Considering option with AVX connectors away from z=0 to facilitate assembly

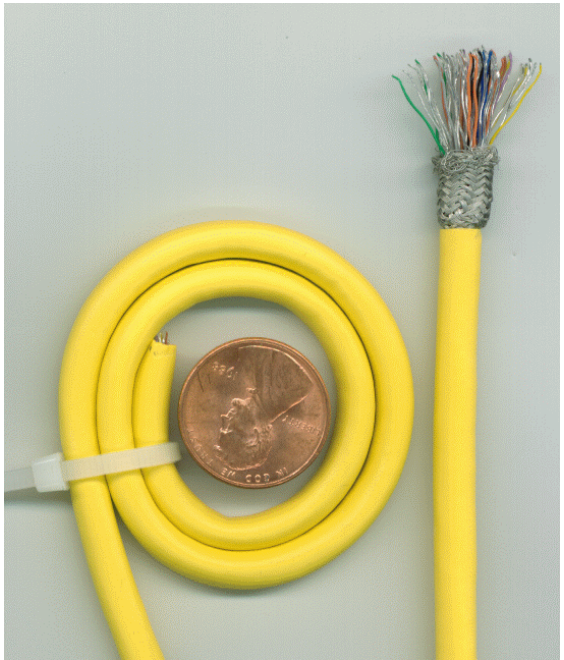


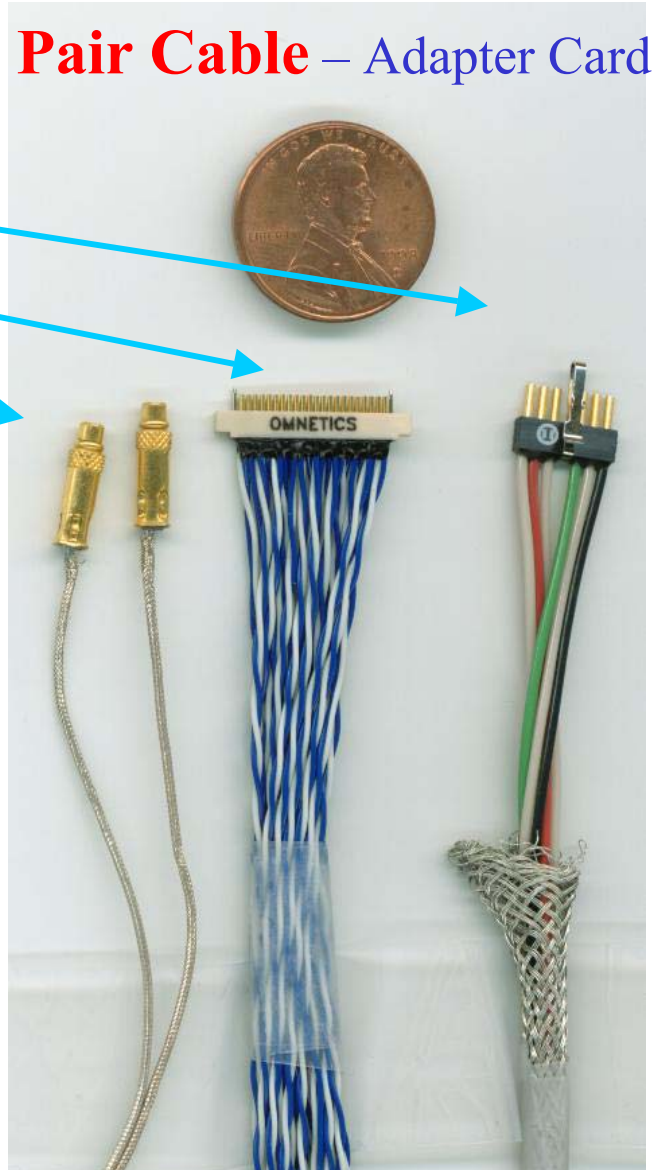


Twisted Pair Cable

Hybrid - Jumper Cable - Junction Card - **Twisted Pair Cable** – Adapter Card

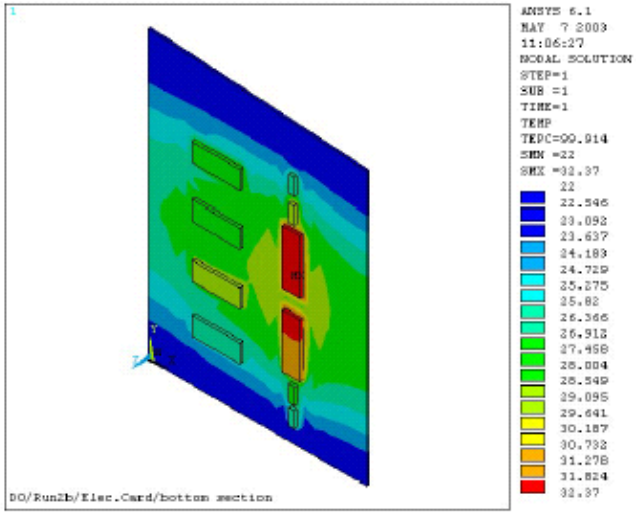
- **Consists of**
  - Power & HV lines : 6-pin Omnetics connector
  - Signal pairs : 44-pin Omnetics connector
  - Clock coaxes
- **Ordered new signal twisted pair cable**
  - Terminated on both sides

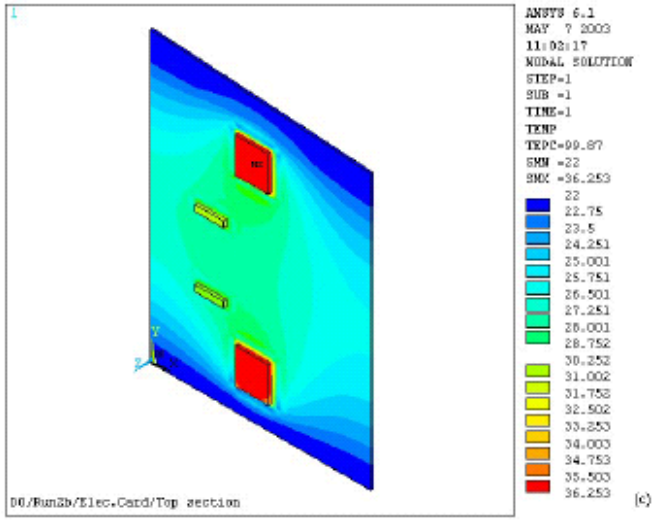




Adapter Card

- Rev.2 Adapter Card discussed at KSU meeting in April, see details in
  - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/AdapterCard/Run%202b_KSU_electronics_21apr03.pdf
- Temperature analysis done (Rafael S, Bill C, Ang L)
  - max Delta T 12 degC – looks acceptable
  - See details here
    - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/AdapterCard/2b_Adapter_Card_Temp.pdf





- Sorting out last details on the power connector

Low & High Voltage

- Received and testing WIENER LV PS (Lynn B, John F), see
  - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/lv/LV_PS_Status_LB032403.pdf
- AC power will go through 80-conductor cable, see
  - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/lv/ACLVPS_scenario5.pdf
- HV supplies : order placed (at last!) with Bira

Production Test Stands

Hybrid - Jumper Cable - **Purple Card** - SASEQ

- Receiving all rev.3 Purple Card by end May 2003 (Russell T, Tim S, Ron S, Eckhard vT)
  - 60 assembled cards at KSU, testing started
- Burn-in stands & Teststations are almost ready (Sasha L, Gustavo O, Cecil N),
  - All infrastructure ready
  - Passed Safety Review
  - Still waiting for rest of Purple Cards & Software

Vertical slice tests

1. Full chain tests with SASEQ (Sergey B, Kristian H, AN)
   - Lots of measurements for rev.2 prototypes
   - Error free readout of 5 M events achieved
   - See more
     - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/FullChain/sl20030414.pdf
     - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/FullChain/fullchain_SB033103.pdf
     - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/FullChain/harder_030421.pdf
2. 1% stand (Lynn B, Dave B, Mike U, Daniel M, Harald F, Stu F)
   - Infrastructure ready
   - Recent progress with firmware but still corruptions at 1% level, see
     - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/Teststand/1percent_teststand_051203.pdf
   - Software in progress (Doug Ch)
3. 10% stand (Lynn B)
   - Infrastructure in progress

Schedule

- Coming Production Readiness Reviews

Silicon

Element/System	Scheduled Date ('03)	Comments
L0 & L1 sensors	May 09	In preparation, same Committee as for L2-5
Low voltage system	Jul 08	
Layer 0 & 1 mechanical structures	Jul 08	In preparation
High voltage system	Aug 01	
Stave design	Aug 08	
L0/1/2 hybrids	Aug-Oct	Will be consolidated
Analog cables	Oct 26	
L0/1/2 digital jumper cables	Sep-Oct	Will be consolidated